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Reviews on Algorithms and Architectures for Efficient Design of MIMO Accelerator

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Abstract

We surveyed about the design techniques of Multiple Input Multiple Output (MIMO) accelerator.The MIMO accelerator is a software programmable device that specializes in MIMO decoding and MIMO signal processing for Orthogonal Frequency Division Multiplexing systems(OFDM).It allows various algorithms to be easily implemented with a single hardware design. The accelerator is fully programmable within the domain of algorithms and functions needed to implement MIMO decoding for any arbitrary system or standards (i.e.,WiFi, LTE, etc.).To improve the system performance and reduce the complexity of the accelerator design some algorithms and architectures has been discussed here. The implementation of Field Programmable Gate Array(FPGA) architectures has been reviewed to minimize the overall energy/area consumption for the efficient design of accelerator hardware.

Keywords:Multiple Input and Multiple Ouput Accelerator,Field Programmable Gate Array.

Introduction

Multiple-input–multiple-output (MIMO) processing and orthogonal frequency division multiplexing (OFDM) are two dominant technologies in emerging wireless communications systems. MIMO transmission increases the capacity and reliability of a wireless system without increasing its bandwidth. OFDM divides a wideband channel into multiple narrowband subchannels via computationally efficient fast Fourier transform (FFT) operation, but it requires identical baseband processing for each of the subchannels. Multiple standards rely on MIMO-OFDM to provide high spectral efficiency and to enable broadband communication.The MIMO decoder is one of the most complex blocks in a MIMO transceiver; it inverts a channel matrix with a low-latency requirement for each subcarrier. A MIMO decoder design process for a certain application is hard and time consuming. This motivates the need for a programmable accelerator block to implement the MIMO decoder and a fast and easy application driven MIMO decoder design flow.The MIMO accelerator chip implementation and hardware test results, highlighting some of the tradeoffs and implementation decisions that affected the hardware cost and performance. A VLSI implementation of the accelerator is introduced highlighting some of the implementation decisions and techniques to minimize the overall energy consumption of the accelerator hardware.

With new wireless communication standards and new MIMO decoding algorithms emerging every few years, existing systems need to be redesigned and upgraded not only to meet the newly defined standards, but also to allow integration of multiple standards onto the same platform and improve performance via more advanced decoding algorithms. This fact serves as the main motivation for the proposed solution. A programmable hardware solution focused on the unique MIMO decoding operations of a MIMO system can help drive down nonrecurring engineering costs, can facilitate system upgrades to take advantage of emerging algorithms and can help minimize hardware duplications in system-on-a-chips (SoCs) that support multiple standards. Through sacrificing part of the performance and/or cost constraints, a multimode MIMO decoder can be designed to target multiple communicationStandards.

The remainder of this paper is structured as following.At first, we illustrate the basic operation of MIMO Accelerator and the data stoarage units used in designing the core memory.Further we present the different rotation algorithms which are used in minimizing the iterations,delay,power and increasing the speed of the Processor.

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MIMO accelerator

The MIMO accelerator is a complex number vector-based processor that works on complex vector operands of length Nrx —where Nrx is the number of receive antennas used in the MIMO system. The basic building blocks of the MIMO accelerator are shown in Fig. 1. The processing core, which is the main data path of the MIMO accelerator, specifically targets the MIMO decoding tasks. It consists of four powerful processing units that are chosen based on the minimum set of primitive operations needed to fully implement most (if not all) MIMO decoding algorithms.

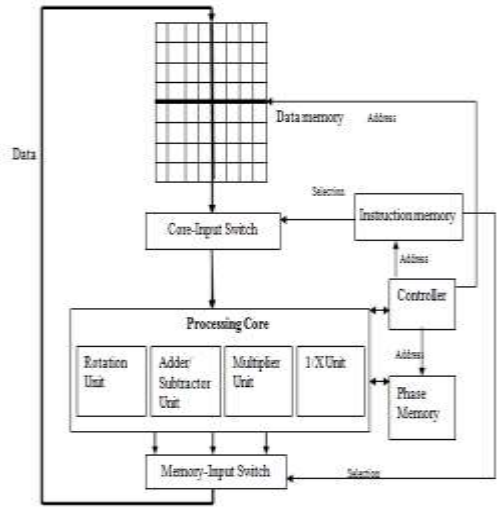

Figure. 1. MIMO accelerator basic diagram

The Figure.1 shows a simplified block diagram of a MIMO accelerator.This accelerator depends on an instruction memory to store predecoded instructions and a data memory.

In the MIMO accelerator the rotation unit is important unit which consumes more area and power compared to other units.The accelerator designed to implement in the decoder side for processing the chosen decoding algorithm with the specified parameters.Based on the design of accelerator the decoding process speed will increased with accuracy.

The accelerator can support different types of decoding algorithms such as Minimum Mean Square Error (MMSE),Maximum Likelihood (ML) and Zero Forcing(ZF) linear decoders with the help of algorithms used in the accelerator architecture.

This architecture is further modified to support variable number of antennas, i.e., for2x2, 3x3, and 4x4 MIMO systems.

Memory access

A.Memory partitioning,Addressing and Vector Operands

Memory read or write operations must be performed as fast as possible since the processing cores are deeply pipelined and provide a new output every processor cycle. Read and write operations can be simultaneously supported through the use of dual port memories, but the randomness of access to matrix elements and the large number of operands needed every cycle require more than multiple-port memories .

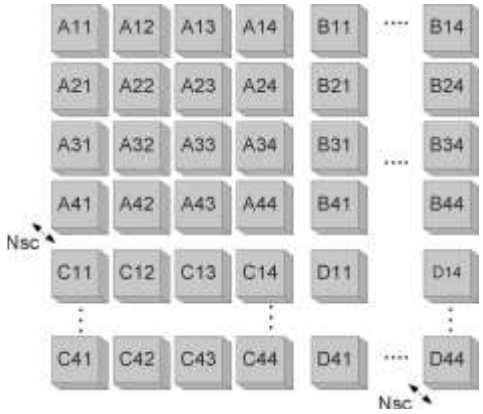

Figure. 2.Memory map

The 4×4 matrix memory map is shown in Figure.2.The four conceptual 4×4 matrices are labeled A, B, C, and D, respectively; and the 64 independent memory blocks (not all shown) are each as deep as the number of subcarriers(N_{sc}).

B. Sorting Circuits and Addressing

Data memory provides access to all elements of a matrix in a fixed, predetermined manner. The processing unit inputs are also fixed, for example, the multiplication core multiplies all elements in input vector 1 with the exact corresponding elements of vector input 2, and the coordinate rotation core always considers the first element to be the vectoring element.

The sorting circuits proved to be two of the most resource intensive components of the MIMO accelerator. Essentially, each sorting circuit consists of a collection of multiplexers equal to the number of target ports (32 for processor input sorter, 64 for memory input sorter), with a number of inputs equal to the source (8 for memory input sorter, 64 for processor input sorter).

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We need to be able to map any of the 64 memory output ports (Fig. 2) to any of the 32 input ports of the processor N1–N32, and any of the eight output ports of the processor to any of the 64 input ports of the memory M1–M32. Alternatively, sorting can be performed at the data memory ports by using memory addresses to access specific elements. Since the memory address is already reserved for indexing the subcarrier, additional addressing for sorting involves some redundancy. Due to the critical nature of the sorting circuits, we considered three alternatives that tradeoff multiplexer use and redundancy in data memory.Altenative approachs to reduce the memory blocks using replication and multiple ports.

Rotation algorithms and architectures

The coordinate rotation digital computer (CORDIC) algorithm is widely used in various technological fields such as communication systems,digital signal processing (DSP), robotics, image processing etc.Using the simple shift and add operations, the use of CORDIC based systems is increasing.The algorithms which are used to reduce the number of iterations reviewed as follows.

A. CORDIC Algorithm

The design shown in Figure 3 uses word-wide data paths.It is called a bit-parallel design.The bit-parallel variable shift shifters do not map well to FPGA architectures because of the high fan-in required.

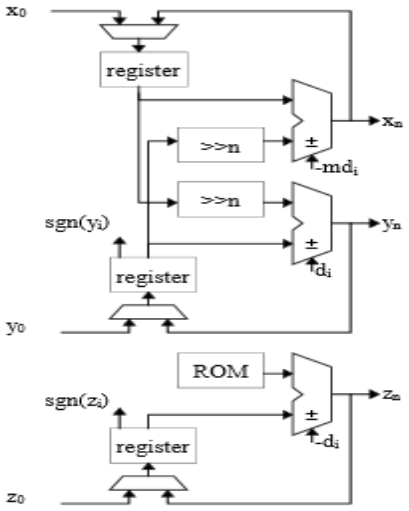

Figure. 3. Iterative cordic

If implemented, those shifters will typically require several layers of logic (i.e., the signal will need to pass through a number of FPGA cells).The design that uses a large number of logic cells which makes the result slow.A considerably more compact design is possible using bit serial arithmetic. The simplified interconnect and logic in a bit serial design allows it to work at a much higher clock rate than the equivalent bit parallel design.

The design also needs to clocked w times for each iteration where w is the width of the data word. The bit serial design consists of three bit serial adder-subtractors, three shift registers and a serial Read Only Memory.

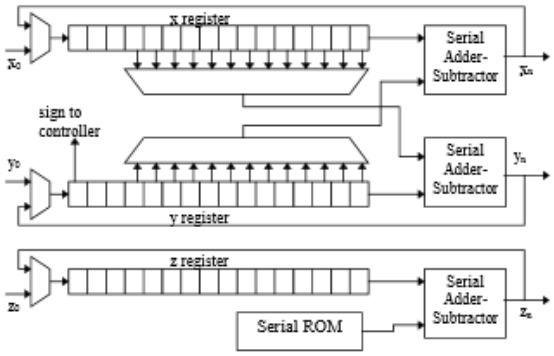

Figure. 4. Bit serial Iterative cordic

Each shift register has a length equal to the word width. There is also some gating or multiplexers to select taps off the shift registers for the right shifted cross terms.The shifting is accomplished using bit delays in bit serial systems. The bit serial CORDIC architecture is shown in Figure 4. In this design, W clocks are required for each of the n iterations, where w is precision of the adders. This iteration design occupies approximately 20% of the FPGA and runs at bit rates up to125 Mhz.

B. Scaling-Free Micro-Rotation Based Circular CORDIC Algorithm

The proposed Scaling-free Micro-rotation based CORDIC algorithm completely eliminates the scale factor of multiplication. By employing the Taylor series expansion of sine and cosine in circular path. the multiplication of the scale factor is removed. The accuracy of the result is based on the selection of the order of approximation of Taylor series, the proposed method takes third order approximation which meets the accuracy requirement and attains the desired range of convergence.

Also an algorithm suggested that redefine the elementary angles with high speed most significant-1 detection for reducing the number of CORDIC iterations. The generalized micro-rotation sequence

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selection technique is suggested to reduce the number of iterations for low latency implementation.

The scaling free cordic algorithm has less time delay and utilizes less number of slices on the Xilinx Vertex XC4VFX12 device.

Table.1.Comparison table for Scaling free cordic.

	Conventional Cordic	**Scaling Free Cordic**
No of slices and Flipflop	26%,5%	17%,8%
No of 4 input LUTs	24%	99%
Minimum input arrival time before clock	4.557ns	3.135ns
Maximum output required time after clock	6.280ns	3.793ns
Total Path delay	7.547ns	3.793ns
Maximum Frequency	233.56MHz	334.353

C.Scale-Free CORDIC Algorithm

The conventional CORDIC algorithm modified to reduce its latency and area.The proposed CORDIC algorithm is completely scale-free for the range of convergence that spans the entire coordinate space. The linear CORDIC processor is replaced by a shift-add network which drastically reduces the number of pipelining stages required in the existing design. The new cordic design on an average requires approximately 64% less pipeline stages and saves up to 44.2% area.The desired angle of rotation is expressed as,

$$\theta = \sum^{for\ an\ iteration} 2^{-ri},\ r_{\min} \le ri \le (N-1) \qquad (1)$$

where *r*min is minimum shift-index, *N* is word length.

A circular CORDIC processor for word lengths up to 16 bits redesigned to scale-free CORDIC processor.It uses third order of approximation of Taylor series to realize scale-free CORDIC iterations.The removal of scaling factor comes with the disadvantage of complex coordinate calculation. Using the priority encoder the micro rotation sequence generation is optimized then the total CORDIC processor pipeline reduced to seven stages.

The area of conventional circular CORDIC processor is calculated using Xilinx CORDIC IP v3.0. The Xilinx CORDIC Core is optimized for circular CORDIC computation with maximum pipelining for 16 bit word length.The gate count is 20122.

The complexity of 16 bit scaling free CORDIC is computed to be equivalent to 1000 one bit full adders and 597 one bit registers.For implementation the area complexity approximately uses 16776 gates.The latency of conventional circular CORDIC is 32 stages,with scaling free it reduced to 28 stages.

D.Pipelined CORDIC Architecture

The CORDIC algorithm using bit serial architecture with all iterations executed in the same hardware slows down the computational device and it is not suitable for high speed implementation.

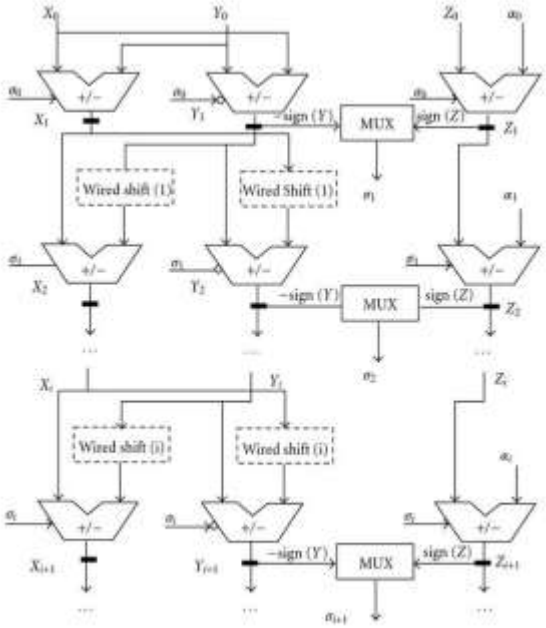

Figure. 5. Pipelined CORDIC

The **Pipelined Architecture**, cascade the iterative CORDIC, which means rebuilding the basic CORDIC structure for each iteration.Consequently, the output of one stage is the input of the next one, as shown in Figure. 5, and in the face of separate stages two simplifications become possible.

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First, the shift operations for each step can be performed by wiring the connections between stages appropriately.Then, there is no need for changing constant values and those can therefore be hardwired as well.Input values find their path through the architecture on their own and do not need to be controlled. This is help to reduce the number of resources and also the latency of computation.

E.Adaptive Cordic Rotator Algorithm(ACRA)

This ACRA algorithm operates in the circular coordinate system and has an unlimited angular convergence range. The algorithm adaptively selects the appropriate iteration steps and thus converges to the target angle executing a minimum number of iterations. On average, the number of iterations 50% less compared to the conventional CORDIC.The adaptive selection of the iteration steps scale factor is virtually constant. The number of adders is reduced by 22%, and 53% fewer registers are needed. Moreover, the hardware requirement for the sign/domain detection circuitry is very small compared to that used for other argument reduction techniques. Based on this algorithm, a 16-b pipelined CORDIC processor core was designed using IHP in-house 0.25-µm BiCMOS technology. The cell area of the CORDIC processor core is equivalent to 24.7 k inverter gates. The latency of the processor is 14 clock cycles. The power consumption of the CORDIC core reported by the synthesis tool is 7mW. The processor is suitable for high-speed low-power applications. Currently, this CORDIC is used in an OFDM baseband processor for a wireless modem compliant with IEEE 802.11.

F.Parallel CORDIC Algorthim(P-CORDIC)

The parallel CORDIC rotation algorithm in circular and hyperbolic coordinate proposed the most critical path of the conventional CORDIC rotation lies within the determination of rotation directions,that depends on the sign of the remaining angle when completion of every iteration. Using the binary to bipolar recoding and microrotation angle recoding techniques, the rotation directions are predicted directly from the binary value of the initial input angle. The original sequential CORDIC rotations can be divided into twophases where the rotations in each phase can be executed in parallel.The critical path delay is reduced using multioperand carry-save addition for micro rotations. At the end of second half iterations,the speed is increased.

The P-CORDIC architecture proposed in a precomputation based rotation CORDIC algorithm. The architecture for X/Y microrotations is the same as conventional CORDIC.The ROM of exponentially increasing area used to store the precomputed values that are required to generate rotation directions. The delay is expressed as,

$$\text{Delay}=(1.625B+B/12+\log_2 B+1)\times T_{FA} \qquad (2)$$

Where B is number of bits and T_{FA} delay in units.For lower bit accuracy(B<32), a $2^{[B/3]}$-entries ROM is required and to generate the rotation directions. For higher bit accuracy (B>32), the ROM size entries reduced to $2^{[B/5]}$-entries with 2B-bit outputs.
The total area required is

$$[(2^{B/3}+2B/8)x0.5)]+B(\log_2 B)+ (0.5B^2+B)x0.4+4B^2]A_{FA.} \qquad (3)$$

The area of one byte ROM takes about 3.5 gates, which is equivalent to using 0.35 CMOS technology.The parallel cordic increase the processing speed.

G.Vectoring and Rotation Cordic Algorithm

K. Mohammed and B. Daneshrad[1] proposed the Energy Efficient Programmable MIMO Decoder Accelerator using the super vectoring Cordic and the super rotation Cordic are used to design the rotation unit.The rotation CORDICs designed without phase interpretation components, instead of using acommon pair of phase processing units that do the job for all 12 rotation CORDICs. This reduces the total resources of the rotation core by 8.7%.The accelerator was fabricated in 65-nm CMOS technology and occupies a core area of 2.48 mm2**.** The power consumption of chip measuredto be 300.9 mW at a clock frequency of 166-MHz clock frequency off of a 1-V supply.

Conclusion

This review article illustrates the various CORDIC algorithms which using reduced number of iteration.This cordic based algorithms used to increase the system performance with less power consumption and latency.This algorithm based processor minimized the core area of the architecture.We have reviewed the FPGA implementation for the various architectures and the applications of CORDIC algorithms ranging from digital signal processing to wireless communication.

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Author Biblography

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